REMARKS

Claims 18-27 are pending in the present application. Claims 18, 26 and 27 have been amended.

Claim Rejections-35 U.S.C. 102

Claims 18-27 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Blanchard reference (U.S. Patent No. 4,767,722). This rejection is respectfully traversed for the following reasons.

The non-volatile memory array of claim 18 includes in combination a first doping region; a second doping region; a third doping region; a fourth doping region; a gate dielectric layer "formed on a surface of the first doping region, an upper surface of the second doping region and a sidewall of the trench, wherein the gate dielectric layer comprises at least one nitride film"; and a conducting plug formed in the trench, "wherein the first doping regions of the vertical transistors are connected as a common plate serving as one of a common source and a common drain". Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose these features.

The Examiner has interpreted gate dielectric layer 32 in Figs. 3 and 6 of the Blanchard reference as the gate dielectric layer of claim 18. However, gate dielectric layer 32 in Figs. 3 and 6 of the Blanchard reference is illustrated as formed within the trench, not on an upper surface of N^+ regions 21a and 21b (interpreted by the Examiner

as the second doping region), as would be necessary to meet the features of claim 18. That is, in Fig. 3 of the Blanchard reference, respective contacts 18 and 19 are formed on the upper surface of regions 21a and 21b. In Fig. 6 of the Blanchard reference, silicon dioxide layer 30 is formed during the source drive-in on the upper surface of regions 21a and 21b, as described in column 3, lines 57-60. Accordingly, the Blanchard reference as relied upon by the Examiner does not disclose a non-volatile array having vertical transistors including in combination a gate dielectric layer formed on an upper surface of a second doping region, as would be necessary to meet the features of claim 18. Applicant therefore respectfully submits that the non-volatile memory array of claim 18 distinguishes over the Blanchard reference as relied upon, and that this rejection, insofar as it may pertain to claims 18-27, is improper for at least these reasons.

With further regard to this rejection, the Examiner has asserted that column 4, lines 54-60 of the Blanchard reference describes a common plate as featured in claim 18. However, column 4, lines 54-60 of the Blanchard reference merely describes that when the gate-to-source potential is sufficiently high and when a positive potential is applied to drain 17 as shown in Fig. 3, electrons flow vertically from N^+ source regions 21a and 21b through channel regions 22c1 and 22c2 and body regions 20a and 20b respectively, and continue to flow vertically downward through drain 11 and N^+ substrate (drain) 10 to drain contact 17. This merely indicates the current flowing path in the vertical direction from source to drain. This particular portion of the Blanchard

reference as relied upon does not describe that the first doping regions of the vertical transistors are a common plate connected as a common source or drain, as featured in claim 18. The cross-sectional views of the single transistor in respective Figs. 3 and 6 do not illustrate plural first doping regions as a common plate of vertical transistors. Applicant therefore respectfully submits that the non-volatile memory array of claim 18 distinguishes over the Blanchard reference as relied upon, and that this rejection, insofar as it may pertain to claims 18-27, is improper for at least these additional reasons.

Claim 26, as dependent upon claim 18, features that "each of the vertical transistors further comprises insulation blocks formed on surfaces of the first and second doping regions". The Examiner has characterized layers 30 and 35 as the insulation blocks of claim 26. Applicant respectfully submits that the Examiner's interpretation is improper for at least the following reasons.

Although Applicant does not necessarily concede that layers 30 and 35 in Fig. 6 of the Blanchard reference may properly be interpreted as an insulation block, it is clear that layers 30 and 35 in Fig. 6 of the Blanchard reference are not formed on a surface of N^+ region 10 (interpreted by the Examiner as the first doping region of claim 18), as would be necessary to meet the features of claim 26. Applicant therefore respectfully submits that the non-volatile memory array of claim 26 distinguishes over the Blanchard reference as relied upon, and that this rejection, insofar as it may pertain to claims 26 and 27, is improper for at least these additional reasons.

Claim 27, as dependent upon claim 26, features that "each of the vertical transistors further comprises edge insulation layers formed on sidewalls of the trench, and the insulation blocks are thicker than the edge insulation layers". Applicant respectfully submits that the Blanchard reference as relied upon by the Examiner does not disclose these features.

The Examiner has apparently also interpreted layers 30 and 35 in Figs. 5 and 6 of the Blanchard reference as edge insulation layers of claim 27, in addition to interpreting layers 30 and 35 as the insulation blocks as featured in claim 26. It is not clear how the same layers may be interpreted as two respectively different claimed features in this case. Regardless, layers 30 and 35 in Figs. 5 and 6 of the Blanchard reference are not formed on sidewalls of the trench, as would be necessary to meet the features of claim 27. That is, gate dielectric layer 32 is formed on sidewalls of the trench in Figs. 5 and 6 of the Blanchard reference. The Blanchard reference thus fails to disclose edge insulation layers as would be necessary to meet the features of claim 27. Also, since the Blanchard reference as relied upon does not disclose edge insulation layers, the Blanchard reference clearly fails to disclose insulation blocks that are thicker than edge insulation layers, as would be necessary to meet the further features of claim 27. Applicant therefore respectfully submits that the non-volatile memory array of claim 27 distinguishes over the Blanchard reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 27, is improper for at least these additional reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

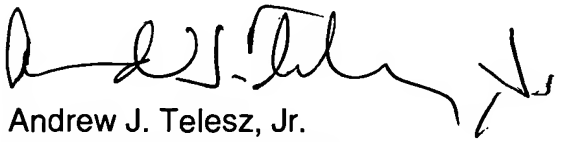
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of three (3) months to June 19, 2006, for the period in which to file a response to the outstanding Office Action. The required small entity fee of $510.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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